ABSTRACT OF THE DISCLOSURE

In a semiconductor memory device which is intended to have a smaller sense amplifier forming area to match with small-sized bit lines, first bit lines BL (e.g., BL2a) are formed on a first layer, and lines M2 (e.g., M2a) are formed on a second layer and connected to the first bit lines in a first connecting area located between a first memory cell area and a sense amplifier area. Second bit lines BL (e.g., BL1c) are formed on the first layer, and lines M2 (e.g., M2c) are formed on the second layer and connected to the second bit lines in a second connecting area located between a second memory cell area and the sense amplifier area. As a result, the lines M2 on the second layer can have a smaller line interval.